

EAST - [9039.wsp.1]

File View Edit Tools Window Help

Active

- L3: (41992) (dielectric insulat\$3) with (photoresist photo adj resist mask\$3)
- L5: (27707) 3 and ((dielectric insulat\$3) with (trench hole via groove opening))
- L6: (13913) 5 and ((dielectric insulat\$3) with ((etch\$3 stop\$4) near3 layer))
- L7: (13913) 6 and ((etch\$3 stop\$4) near3 layer)
- L8: (1567) 7 and ((spacer) near5 (trench hole via groove opening))
- L9: (1368) 7 and ((spacer) near4 (trench hole via groove opening))
- L10: (1139) 7 and ((spacer) near3 (trench hole via groove opening))
- L11: (769) 7 and ((spacer) near2 (trench hole via groove opening))
- L12: (285) 7 and ((spacer) near (trench hole via groove opening))
- L13: (285) 12 and (spacer trench hole via groove opening dielectric mask\$3 photoresist resist)
- L14: (285) 13 and ((etch\$3 stop\$4) near3 layer)
- L15: (114) 13 and (etch\$3 near3 stop\$4)

13 and (etch\$3 near3 stop\$4)

	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRel
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20040014310 A1	20040122	9	Method for producing an integrated circuit	438/622	438/631; 438/636;
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20040012009 A1	20040122	19	Sublithographic contact structure, phase change memory cell with optim	257/4	257/5; 438/409
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20040002212 A1	20040101	13	Method for forming copper metal line in semiconductor device	438/687	438/631; 438/634
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20030231530 A1	20031218	19	Phase change memory cell and manufacturing method thereof using	365/200	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20030223296 A1	20031204	35	Self-aligned method of forming a semiconductor memory array of floati	365/201	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20030214856 A1	20031120	21	Contact structure, phase change memory cell, and manufacturing meth	365/200	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20030214022	20031120	11	Bit line landing pad and borderless	257/678	

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L15: (114) 13 and (etch\$3 near3 stop\$4)								
	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRel
1	<input type="checkbox"/>	<input type="checkbox"/>	US 20040014310 A1	20040122	9	Method for producing an integrated circuit	438/622	438/631; 438/636;
2	<input type="checkbox"/>	<input type="checkbox"/>	US 20040012009 A1	20040122	19	Sublithographic contact structure, phase change memory cell with optim	257/4	257/5; 438/409
3	<input type="checkbox"/>	<input type="checkbox"/>	US 20040002212 A1	20040101	13	Method for forming copper metal line in semiconductor device	438/687	438/631; 438/634
4	<input type="checkbox"/>	<input type="checkbox"/>	US 20030231530 A1	20031218	19	Phase change memory cell and manufacturing method thereof using	365/200	
5	<input type="checkbox"/>	<input type="checkbox"/>	US 20030223296 A1	20031204	35	Self-aligned method of forming a semiconductor memory array of floati	365/201	
6	<input type="checkbox"/>	<input type="checkbox"/>	US 20030214856 A1	20031120	21	Contact structure, phase change memory cell, and manufacturing meth	365/200	
7	<input type="checkbox"/>	<input type="checkbox"/>	US 20030214022 A1	20031120	11	Bit line landing pad and borderless contact on bit line stud with localized	257/678	
8	<input type="checkbox"/>	<input type="checkbox"/>	US 20030162350 A1	20030828	13	Method for producing a bipolar transistor	438/235	438/309; 438/312;
9	<input type="checkbox"/>	<input type="checkbox"/>	US 20030109090 A1	20030612	17	Intrinsic dual gate oxide mosfet using a damascene gate process	438/197	257/E21.193; 257/E21.339;
10	<input type="checkbox"/>	<input type="checkbox"/>	US 20030068896 A1	20030410	11	Etch aided by electrically shorting upper and lower sidewall portions dur	438/705	
11	<input type="checkbox"/>	<input type="checkbox"/>	US 20030062543 A1	20030403	42	Semiconductor device and its manufacture	257/200	257/E21.019; 257/E21.02
12	<input type="checkbox"/>	<input type="checkbox"/>	US 20030048679 A1	20030313	40	Methods of forming contact holes using multiple insulating layers and int	365/200	
13	<input type="checkbox"/>	<input type="checkbox"/>	US 20020187648 A1	20021212	85	Material removal method for forming a structure	438/745	257/E21.011; 257/E21.166;
14	<input type="checkbox"/>	<input type="checkbox"/>	US 20020182872 A1	20021205	85	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
15	<input type="checkbox"/>	<input type="checkbox"/>	US 20020182816	20021205	83	Material removal method for forming	438/345	257/E21.011

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	U	I	Document ID	Issue Date	Pages	Title	Current OR	Current XRel
16	<input type="checkbox"/>	<input type="checkbox"/>	US 20020146897 A1	20021010	17	STRUCTURE HAVING REDUCED LATERAL SPACER EROSION	438/586	257/774;
17	<input type="checkbox"/>	<input type="checkbox"/>	US 20020146891 A1	20021010	14	Method for forming isolation trench	438/437	257/E21.62; 257/E21.549;
18	<input type="checkbox"/>	<input type="checkbox"/>	US 20020123234 A1	20020905	8	Method and composition for plasma etching of a self-aligned contact openi	438/746	438/435 257/E21.546
19	<input type="checkbox"/>	<input type="checkbox"/>	US 20020123226 A1	20020905	8	Method and composition for plasma etching of a self-aligned contact openi	438/698	257/E21.546
20	<input type="checkbox"/>	<input type="checkbox"/>	US 20020119637 A1	20020829	16	Intrinsic dual gate oxide MOSFET using a damascene gate process	438/423	257/530; 257/E21.193;
21	<input type="checkbox"/>	<input type="checkbox"/>	US 20020113675 A1	20020822	40	Movable-body apparatus, optical deflector, and method of fabricating t	335/80	
22	<input type="checkbox"/>	<input type="checkbox"/>	US 20020110992 A1	20020815	12	Use of hydrocarbon addition for the elimination of micromasking during et	438/389	
23	<input type="checkbox"/>	<input type="checkbox"/>	US 20020108929 A1	20020815	10	Use of ammonia for etching organic low-k dielectrics	216/58	
24	<input type="checkbox"/>	<input type="checkbox"/>	US 20020105035 A1	20020808	14	Self-aligned, magnetoresistive random-access memory (MRAM) str	257/375	
25	<input type="checkbox"/>	<input type="checkbox"/>	US 20020024057 A1	20020228	49	Semiconductor device and process of fabricating same	257/155	
26	<input type="checkbox"/>	<input type="checkbox"/>	US 20020017671 A1	20020214	46	Dram cell configuration, and method for producing the dram cell configura	257/301	257/E21.652; 257/E27.096
27	<input type="checkbox"/>	<input type="checkbox"/>	US 20020011608 A1	20020131	33	Self aligned method of forming a semiconductor memory array of floati	257/200	257/E21.682; 257/E27.103
28	<input type="checkbox"/>	<input type="checkbox"/>	US 20020001960 A1	20020103	89	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
29	<input type="checkbox"/>	<input type="checkbox"/>	US 20020000629 A1	20020103	18	MOSFET device fabrication method capable of allowing application of self	257/412	257/344; 257/E21.29;
30	<input type="checkbox"/>	<input type="checkbox"/>	US 20010046753	20011129	21	METHOD FOR FORMING A	438/474	257/E21.551

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31	<input type="checkbox"/>	<input type="checkbox"/>	US 20010028077 A1	20011011	42	Semiconductor device and its manufacture	257/303	257/E21.019; 257/E21.02
32	<input type="checkbox"/>	<input type="checkbox"/>	US 20010024380 A1	20010927	43	Memory cell configuration in which an electrical resistance of a memory el	365/158	
33	<input type="checkbox"/>	<input type="checkbox"/>	US 20010019866 A1	20010906	13	Method of forming a contact hole in a semiconductor substrate using oxide	438/241	257/E21.257; 257/E21.577;
34	<input type="checkbox"/>	<input type="checkbox"/>	US 20010018787 A1	20010906	13	Method for fabricating a capacitor in a semiconductor memory device	29/25.01	216/18; 216/6;
35	<input type="checkbox"/>	<input type="checkbox"/>	US 6661823 B1	20031209	47	Vertical resonator type surface light emitting semiconductor laser device a	372/49	372/43; 372/45;
36	<input type="checkbox"/>	<input type="checkbox"/>	US 6620733 B2	20030916	12	Use of hydrocarbon addition for the elimination of micromasking during et	438/700	438/694; 438/710
37	<input type="checkbox"/>	<input type="checkbox"/>	US 6599840 B2	20030729	82	Material removal method for forming a structure	438/705	257/E21.011; 257/E21.166;
38	<input type="checkbox"/>	<input type="checkbox"/>	US 6596648 B2	20030722	83	Material removal method for forming a structure	438/745	257/E21.011; 257/E21.166;
39	<input type="checkbox"/>	<input type="checkbox"/>	US 6596642 B2	20030722	80	Material removal method for forming a structure	438/705	216/38; 216/87;
40	<input type="checkbox"/>	<input type="checkbox"/>	US 6586795 B2	20030701	44	DRAM cell configuration whose memory cells can have transistors an	257/302	257/303; 257/E21.652;
41	<input type="checkbox"/>	<input type="checkbox"/>	US 6559499 B1	20030506	7	Process for fabricating an integrated circuit device having capacitors with	257/311	257/309; 257/310;
42	<input type="checkbox"/>	<input type="checkbox"/>	US 6544861 B2	20030408	14	Method for forming isolation trench	438/424	257/E21.549; 438/296;
43	<input type="checkbox"/>	<input type="checkbox"/>	US 6537865 B2	20030325	47	Semiconductor device and process of fabricating same	438/172	
44	<input type="checkbox"/>	<input type="checkbox"/>	US 6531410 B2	20030311	16	Intrinsic dual gate oxide MOSFET using a damascene gate process	438/766	257/E21.193; 257/E21.339;
45	<input type="checkbox"/>	<input type="checkbox"/>	US 6521931 B2	20030218	14	Self-aligned magnetoresistive	257/295	257/421

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61	<input type="checkbox"/>	<input type="checkbox"/>	US 6329685 B1	20011211	34	Self aligned method of forming a semiconductor memory array of floati	257/314	257/315;
62	<input type="checkbox"/>	<input type="checkbox"/>	US 6309975 B1	20011030	91	Methods of making implanted structures	438/705	257/316;
63	<input type="checkbox"/>	<input type="checkbox"/>	US 6300238 B1	20011009	8	Method of fabricating node contact opening	438/624	216/38;
64	<input type="checkbox"/>	<input type="checkbox"/>	US 6294801 B1	20010925	47	Semiconductor device with Schottky layer	257/192	216/87;
65	<input type="checkbox"/>	<input type="checkbox"/>	US 6274936 B1	20010814	10	Method for forming a contact during the formation of a semiconductor dev	257/776	257/E21.649;
66	<input type="checkbox"/>	<input type="checkbox"/>	US 6265295 B1	20010724	7	Method of preventing tilting over	438/586	438/639;
67	<input type="checkbox"/>	<input type="checkbox"/>	US 6261964 B1	20010717	91	Material removal method for forming a structure	438/705	257/194;
68	<input type="checkbox"/>	<input type="checkbox"/>	US 6255689 B1	20010703	9	Flash memory structure and method of manufacture	257/314	257/195;
69	<input type="checkbox"/>	<input type="checkbox"/>	US 6255161 B1	20010703	16	Method of forming a capacitor and a contact plug	438/254	257/774;
70	<input type="checkbox"/>	<input type="checkbox"/>	US 6221714 B1	20010424	12	Method of forming a contact hole in a semiconductor substrate using oxide	438/241	257/E21.578;
71	<input type="checkbox"/>	<input type="checkbox"/>	US 6197682 B1	20010306	59	Structure of a contact hole in a semiconductor device and method of	438/639	257/E21.576;
72	<input type="checkbox"/>	<input type="checkbox"/>	US 6191459 B1	20010220	12	Electrically programmable memory cell array, using charge carrier traps a	257/390	438/303;
73	<input type="checkbox"/>	<input type="checkbox"/>	US 6187672 B1	20010213	22	Interconnect with low dielectric constant insulators for semiconductor	438/639	257/E21.011;
74	<input type="checkbox"/>	<input type="checkbox"/>	US 6180517 B1	20010130	11	Method of forming submicron contacts and vias in an integrated circ	438/639	257/E21.166;
75	<input type="checkbox"/>	<input type="checkbox"/>	US 6177600 B1	20010123	26	DRAM cell having a verticle	257/303	257/315;

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76	<input type="checkbox"/>	<input type="checkbox"/>	US 6174763 B1	20010116	36	Three-dimensional SRAM trench structure and fabrication method ther	438/238	257/E21.661;
77	<input type="checkbox"/>	<input type="checkbox"/>	US 6153905 A	20001128	22	Semiconductor component including MOSFET with asymmetric gate electr	257/320	257/E21.703;
78	<input type="checkbox"/>	<input type="checkbox"/>	US 6097076 A	20000801	19	Self-aligned isolation trench	257/513	257/316;
79	<input type="checkbox"/>	<input type="checkbox"/>	US 6096594 A	20000801	11	Fabricating method of a dynamic random access memory	438/238	257/317;
80	<input type="checkbox"/>	<input type="checkbox"/>	US 6091129 A	20000718	44	Self-aligned trench isolated structure	257/510	257/510;
81	<input type="checkbox"/>	<input type="checkbox"/>	US 6087705 A	20000711	9	Trench isolation structure partially bound between a pair of low K dielec	257/510	257/524;
82	<input type="checkbox"/>	<input type="checkbox"/>	US 6074955 A	20000613	9	Method of fabricating a node contact window of DRAM	438/710	257/E21.648;
83	<input type="checkbox"/>	<input type="checkbox"/>	US 6066555 A	20000523	17	Method for eliminating lateral spacer erosion on enclosed contact topogra	438/634	438/252;
84	<input type="checkbox"/>	<input type="checkbox"/>	US 6051456 A	20000418	24	Semiconductor component and method of manufacture	438/202	257/622;
85	<input type="checkbox"/>	<input type="checkbox"/>	US 6043131 A	20000328	7	Method for making a flower shaped DRAM capacitor	438/396	257/E21.206;
86	<input type="checkbox"/>	<input type="checkbox"/>	US 6037202 A	20000314	33	Method for growing an epitaxial layer of material using a high temperature in	438/212	257/501;
87	<input type="checkbox"/>	<input type="checkbox"/>	US 6037194 A	20000314	27	Method for making a DRAM cell with grooved transfer device	438/147	257/644;
88	<input type="checkbox"/>	<input type="checkbox"/>	US 5963279 A	19991005	32	Liquid crystal display device containing openings in a protective la	349/54	257/E21.507;
89	<input type="checkbox"/>	<input type="checkbox"/>	US 5945707 A	19990831	25	DRAM cell with grooved transfer device	257/330	257/E21.577;
90	<input type="checkbox"/>	<input type="checkbox"/>	US 5942803 A	19990824	7	Methods for forming openings with	257/774	257/E21.582;



